CLAIMS:

1. A method of forming a co-axial line comprising:

providing a substrate having an outer surface;

forming a conductive line at least a portion of which is elevationally spaced from the outer surface;

forming a dielectric polymer layer over and surrounding at least a portion of the conductive line where it is spaced from the outer surface; and

forming an outer conductive sheath over the dielectric polymer layer.

2. The method of claim 1, wherein the forming of the outer conductive sheath comprises chemical vapor depositing a metal-comprising layer of material over the dielectric polymer layer.

3. The method of claim 2, wherein the metal-comprising layer includes aluminum.

4. The method of claim 1, wherein the dielectric polymer layer comprises Parylene.

5. The method of claim 1, wherein the forming of the conductive line comprises:

forming a conductive line pattern over the substrate outer surface;

forming conductive material over and within the conductive line pattern; and

removing material of the conductive line pattern from elevationally below the conductive material.

6. The method of claim 5, wherein the forming of the conductive material comprises:

forming a conductive film layer over the conductive line pattern; and

electroplating conductive material over the conductive film layer.

7. The method of claim 5, wherein the forming of the conductive material comprises electroless plating a conductive material over the conductive line pattern.

8. A method of forming a conductive line comprising:

forming conductive material within a line pattern within a layer of photoresist and over a substrate outer surface; and

removing the layer of photoresist and suspending at least a portion of the conductive material in the line pattern above the substrate outer surface.

9. The method of claim 8, wherein the forming of the conductive material comprises electroplating a conductive material over the layer of photoresist.

10. The method of claim 8, wherein the forming of the conductive material comprises electroless plating a conductive material over the layer of photoresist.

11. The method of claim 8, wherein the suspending of the conductive material comprises prior to the forming of the conductive material, forming at least one terminal member over the substrate outer surface, the conductive material being formed over and support by the terminal member.

12. A method of forming a co-axial line comprising:

forming a masking material layer over a substrate;

patterning the masking material layer to form at least one conductive line pattern;

forming an inner conductive layer within the at least one conductive line pattern;

vapor depositing a layer comprising a polymer dielectric material over at least some of the inner conductive layer; and

forming an outer conductive layer over the polymer dielectric material.

13. The method of claim 12, wherein the forming of the inner conductive layer comprises:

sputtering a conductive film layer over the conductive line pattern; and

electroplating a conductive material over the conductive film layer.

14. The method of claim 12, wherein the forming of the inner conductive layer comprises electroless plating a conductive material over the conductive line pattern.

15. The method of claim 12 further comprising prior to vapor depositing the polymer dielectric material, removing at least some of the masking material layer.

16. The method of claim 12, wherein the patterning comprises forming a plurality of conductive line patterns.

17. The method of claim 16 further comprising after forming the inner conductive layer, planarizing the inner conductive layer relative to the masking material layer.

18. The method of claim 16 further comprising:

after forming the inner conductive layer, planarizing the inner conductive layer relative to the masking material layer; and

prior to vapor depositing the polymer dielectric material, removing at least some of the masking material layer.

19. A method of forming a co-axial line comprising:

forming a pair of upstanding, spaced-apart conductive terminal members over a substrate;

forming a co-axial inner conductive line component which extends between and electrically connects with the terminal members;

surrounding a substantial portion of the inner conductive line component with a dielectric polymer layer; and

forming a co-axial outer conductive line component over the dielectric polymer layer.

20. The method of claim 19 further comprising forming a masking material trough which extends between exposed portions of the terminal members, at least a portion of the inner conductive line component being formed within the trough.

21. The method of claim 19, wherein the forming of the co-axial inner conductive line component comprises:

forming a masking material over the substrate;

patterning the masking material to form a conductive line pattern which exposes at least some of the conductive terminal members; and

electrically connecting exposed portions of the conductive terminal members through the conductive line pattern.

22. The method of claim 21, wherein the electrically connecting comprises electroplating conductive material at least within the conductive line pattern.

23. The method of claim 21, wherein the electrically connecting comprises electroless plating a conductive material at least within the conductive line pattern.

24. The method of claim 19, wherein the dielectric polymer layer comprises Parylene.

25. The method of claim 19, wherein the forming of the co-axial outer conductive line component comprises chemical vapor depositing a metal-comprising layer over the dielectric polymer layer.

26. The method of claim 19, wherein the forming of the co-axial outer conductive line component comprises electroless plating the line component over the dielectric polymer layer.

27. A method of forming a co-axial line comprising:

forming a pair of upstanding, spaced-apart terminal members over a substrate;

forming photoresist over the terminal members;

forming a line pattern within the photoresist which exposes and extends between the terminal members;

sputtering a first conductive layer of material over the co-axial line pattern;

electroplating a second conductive material over the first conductive layer;

forming a dielectric layer over the second conductive material surrounding a substantial portion thereof; and

forming an outer conductive sheath of material over the dielectric layer.

28. The method of claim 27, wherein the sputtering of the first conductive layer comprises ionized magnetron sputtering of the first conductive layer.

29. The method of claim 27, wherein the forming of the dielectric layer comprises forming a polymer layer over the second conductive material.

30. The method of claim 27 further comprising after the electroplating of the second conductive material:

planarizing the second conductive material relative to the photoresist; and

prior to the forming of the dielectric layer, removing the photoresist from around the second conductive material.

31. A method of forming a co-axial line comprising:

forming a pair of upstanding, spaced-apart terminal members over a substrate;

forming photoresist over the terminal members;

forming a line pattern within the photoresist which exposes and extends between the terminal members;

electroless plating a conductive material over the co-axial line pattern;

forming a dielectric layer over the conductive material; and

forming an outer conductive sheath of material over the dielectric layer.

32. The method of claim 31, wherein the forming of the dielectric layer comprises forming a polymer layer over the electroless-plated conductive material.

33. The method of claim 31 further comprising after the electroless plating of the conductive material:

planarizing the electroless-plated conductive material relative to the photoresist; and

prior to the forming of the dielectric layer, removing the photoresist from around the electroless-plated conductive material.

34. A method of forming a co-axial line comprising:

providing a substrate having an outer surface;

forming a pair of upstanding, spaced-apart conductive terminal members over the substrate outer surface;

forming a layer of photoresist over the substrate outer surface;

forming a conductive line pattern in the photoresist, the conductive line pattern extending at least between and exposing portions of the conductive terminal members;

forming a layer of conductive material over the substrate and within the conductive line pattern;

removing a sufficient amount of material of the layer of conductive material to electrically isolate the conductive material within the conductive line pattern;

removing photoresist from at least around a conductive material portion which extends between the spaced-apart conductive terminal members, the removing of the photoresist leaving the conductive material portion supported above underlying substrate outer surface;

vapor depositing a polymer dielectric material comprising Parylene, the depositing of the Parylene completely surrounding the conductive material portion which extends between the spaced-apart conductive terminal members; and

vapor depositing a conductive material at least over the Parylene which surrounds the conductive material portion which extends between the spaced-apart conductive terminal members.

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35. Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

an inner conductive core spaced from and over the outer surface;

a polymer dielectric layer surrounding a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

36. Integrated circuitry comprising:

a semiconductive substrate having an outer surface;

a pair of spaced-apart terminal members disposed over the outer surface and extending elevationally away therefrom;

an inner conductive core operably connected with and extending between the spaced-apart terminal members;

a polymer dielectric layer over a substantial portion of the inner conductive core; and

an outer conductive sheath surrounding a substantial portion of the polymer dielectric layer.

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37. Integrated circuitry comprising:

a substrate having an outer surface;

a pair of upstanding, spaced-apart conductive terminal members disposed over the substrate outer surface;

a copper-comprising layer of material operably connected with and extending between the terminal members, the copper-comprising layer having a thickness of between about 100 to 200 nanometers;

a conductive layer of material disposed over and operably connected with the copper-comprising layer of material, the conductive layer comprising conductive material selected from the group consisting of copper, gold, nickel, cobalt, and iron;

a dielectric layer comprising Parylene disposed over the conductive layer of material, the dielectric layer surrounding conductive layer portions which extend between the terminal members; and

an outer conductive sheath of material disposed over the dielectric layer and surrounding dielectric layer portions which extend between the terminal members.

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